Design of Phase-Frequency Detectors (PFD), Charge Pumps, and Loop Filters

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Outline

• Phase Detector (PD)
• Phase-Frequency Detector (PFD)
• Charge Pump
• Loop Filter

Phase Detector

• Performs Phase Comparison for Reference and Prescaler’s Output
• Key Parameters
  – Phase Comparison Range
  – Gain
  – Noise and Spur
• Typically Digital and Operate on Edges of Inputs
• Fast Transition Edges Can Be Achieved

Analog Phase Detector

• Can Be Implemented Using a Simple Mixer
• Compared to Digital Counterparts:
  – Input Can Be Sinusoidal
  – Can Operate at Much Higher Frequencies
  – Input Amplitude Affects Output, Gain, PLL Loop Gain and Dynamic Behavior
  – Larger Power Consumption

\[ f_{\text{ref}} \xrightarrow{\bigtriangleup} v_{PD} \xrightarrow{f_{\text{div}}} \]
XOR Phase Detector

- Simple
- Gain Independent of Input Amplitude
- Require Square-Wave Inputs
- Locked-State Input Phase Error is 90 Degrees => Nominal Duty Cycle of 50%
- Output Frequency is Twice Reference

\[ f_{\text{div}} \]

\[ f_{\text{ref}} \]

\[ V_{PD} \]

\[ f_{\text{ref}} \]

\[ f_{\text{div}} \]

\[ V_{PD} \]

\[ \phi_e = \phi_{\text{ref}} - \phi_{\text{div}} \]

\[ <V_{PD}> = -1 + 2 \frac{W}{T} \]

\[ W = \frac{\phi_e}{\pi} T \]

\[ <V_{PD}> = -1 + 2 \frac{|\phi_e|}{\pi} \]

XOR Phase Detector - Gain

- DC Characteristic is Defined as Average of Output \(<V_{PD}>\) as Function of Input Phase Error \(\phi_e\)
- Gain = Slope of DC Characteristic Curve
- Sensitive to Both Rising and Falling Edges of Reference and Divider Output

\[ \phi_e = \phi_{\text{ref}} - \phi_{\text{div}} \]

\[ V_{PD} \]

\[ \frac{1}{T/2} \]

\[ t \]

\[ <V_{PD}> = -1 + 2 \frac{W}{T} \]

\[ W = \frac{\phi_e}{\pi} T \]

\[ <V_{PD}> = -1 + 2 \frac{|\phi_e|}{\pi} \]

XOR Phase Detector - Gain

- Gain Has Sign Inversion for An Increment of Phase Error of 180 Degrees
- Consequently, Usable Phase Range is 180 Degrees
- Locked-State Phase Error is 90 Degrees
- PD Gain:

\[ K_{PD} = \frac{2}{\pi} \]
XOR Phase Detector with Extended Range

- Modified to be sensitive to only rising or falling edges

\[ \frac{f_{\text{ref}}}{2} \quad \div 2 \quad \frac{f_{\text{div}}}{2} \]

\[ V_{\text{PD}} \]

XOR Phase Detector with Extended Range

- Output frequency is same as reference

\[ <V_{\text{PD}}> \]

\[ -2\pi \quad 2\pi \]

\[ -1 \quad 1 \]

\[ \phi_e \]

XOR Phase Detector with Extended Range

- Gain Has Sign Inversion for An Increment of Phase Error of 360 Degrees
- Consequently, Usable Phase Range is 360 Degrees
- Locked-State Phase Error is 180 Degrees
- PD Gain:

\[ K_{PD} = \frac{1}{\pi} \]

XOR Phase Detector - Limitation

- Frequency Acquisition Can Be Slow
- Input Square Waves Required for Digital Phase Detectors => High Harmonics
- Divider Output Can Lock to Reference Harmonics Unless VCO Output Frequency Range is Limited
- Solution: Phase-Frequency Detection
Phase-Frequency Detector (PFD)

Phase-Frequency Detector (PFD) – Timing Diagram

Phase-Frequency Detector (PFD)

Phase-Frequency Detector (PFD)

• Tri-state PFD
• Edge-Triggering Circuits Are Used to Eliminate Dependency of Gain to Input Duty Cycle
• Nominal Output Frequency is Same as Reference
• Two Outputs are Subtracted => Output Has Three Possible States: –1, 0, 1
• Locked-State Phase Error is 0 Degree => Small Pulses at Outputs => Low Power, Low Noise
Phase-Frequency Detector (PFD)

\[ K_{PD} = \frac{1}{2\pi} \]

- Sign of output (Up – Down) is same as phase error \( \Rightarrow \) frequency detection
- Usable phase range is extended to \( 4\pi \)

Phase-Frequency Detector Without Dead Zone

- When Phase Error is Too Small, PFD Cannot Compare, and Output Become Zero \( \Rightarrow \) Dead Zone \( \Rightarrow \) Phase Noise from Reference and VCO are NOT Suppressed \( \Rightarrow \) Poor Close-In Phase Noise

\[ \text{Delay Added to Remove Dead Zone} \]
Phase-Frequency Detector Without Dead Zone

- Add Delay in Reset Path Which Sets Minimum Pulse Width
- Remove Dead Zone => Improve PFD Gain Linearity
- Generate Pulses for both Up and Down => Increase Power and Noise

PFD Model

\[ \phi_{\text{ref}} \rightarrow \text{PFD} \rightarrow \phi_{\text{div}} \]

- For XOR-based:
  \[ K_{PFD} = \frac{1}{\pi} \]
- For tri-state PFD:
  \[ K_{PFD} = \frac{1}{2\pi} \]

Charge-Pump Phase-Locked Loop

- Employs A Phase-Frequency Detector (PFD) and a Charge Pump (CP) instead of a Phase Detector (PD)

Charge-Pump Phase-Locked Loop

- Transfer Function of PFD and Charge Pump Has a Pole at Zero (Integrator)
- Together with Another Pole at Zero from VCO, PLL System May Be Unstable
- To Ensure Stability, A Zero is Added by Including Resistor \( R_z \) in Series with \( C_z \)
- In Practice, A Capacitor \( C_p \) is Connected in Parallel to Suppress Ripples at \( V_C \), which Would Introduce A Third Pole
Charge-Pump Phase-Locked Loop

\[ K_{PFD} = \frac{I_{CP}}{2\pi} \]
\[ G_{LPF}(s) = \left( R_z + \frac{1}{C_z s} \right) \]
\[ H_{ref}(s)\bigg|_{close} = \frac{K_{PFD}(s)G_{LPF}(s)K_{VCO}}{s + K_{PFD}(s)G_{LPF}(s)K_{VCO}} \]
\[ = H_o \frac{(s + \omega_z)}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]

Charge-Pump Phase-Locked Loop

\[ \therefore H_o = \frac{I_{CP} R_z}{2\pi K_{VCO}} \]
\[ \omega_z = -\frac{1}{R_z C_z} \]
\[ \therefore \omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi C_z}} \]
\[ \zeta = \frac{\omega_n R_z C_z}{2\pi} = \frac{\omega_n}{2\omega_z} \]
\[ \therefore \zeta \omega_n = \frac{I_{CP} R_z}{4\pi} K_{VCO} \]

Charge-Pump Phase-Locked Loop (CPPLL)

- Natural Frequency \( \omega_n \) Does Not Depend on \( R_z \)
- Both \( \omega_n \) and \( \zeta \) Can Be Maximized Simultaneously by Increasing \( I_{CP} \) or \( K_{VCO} \)
- Time Constant \( (\zeta \omega_n) \) and Settling Time Do NOT Depend on \( C_z \)

Synthesizer Using Charge-Pump Phase-Locked Loop

\[ K_{PFD} = \frac{I_{CP}}{2\pi} \]
\[ G_{LPF}(s) = \left( R_z + \frac{1}{C_z s} \right) \]
\[ H_{ref}(s)\bigg|_{close} = \frac{K_{PFD}(s)G_{LPF}(s)K_{VCO}}{s + K_{PFD}(s)G_{LPF}(s)K_{VCO}} \]
\[ = H_o \frac{(s + \omega_z)}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]
Sythesizer Using Charge-Pump Phase-Locked Loop

\[ H_o = \frac{I_{cp} R_z}{2\pi} K_{vco}; \quad \omega_z = -\frac{1}{R_z C_z}\]

\[ \omega_n = \sqrt{\frac{I_{cp} K_{vco}}{2\pi C_z M}}\]

\[ \zeta = \frac{R_z}{2} \sqrt{\frac{I_{cp} C_z}{2\pi K_{vco} M}} = \frac{\omega_n R_z C_z}{2} = \frac{\omega_n}{2\omega_z}\]

\[ \zeta \omega_n = \frac{I_{cp} R_z}{4\pi} K_{vco} \frac{1}{M}\]

Charge Pump - Challenges

- Face same problems as sample-and-hold and switched-capacitor circuits:
  - Charge injection
  - Charge sharing
  - Clock feed-through
- Critical to match up and down currents to minimize spur

Charge Pump - Solutions

- Many solutions for sample-and-hold and switched-capacitor circuits can be applied:
  - Dummy transistors
  - Complimentary switches
  - Unit-gain buffers
  - Differential design
- Need to have fast turn-on time => Use current steering technique to keep bias current on all the times
Charge Pump – Dummy Transistors

Charge Pump – Complementary Switches

Charge Pump – Differential Configuration

Charge Pump - Solutions
**Charge Pump – Current Mismatches**

- To minimize current mismatches:
  - Increase channel length and width
  - Employ good layout techniques
  - Maximize $V_{gs}$

\[
\frac{\Delta I}{I} = \frac{\Delta W}{W} + \frac{\Delta L}{L} + 2 \frac{\Delta V_t}{V_{gs} - V_t}
\]

**Charge Pump with Adaptive Current**

- High charge-pump current:
  - Fast acquisition
  - Low stability
  - High phase noise and jitter
- Low charge-pump current:
  - Slow acquisition
  - Good stability
  - Low phase noise and jitter

=> Start with high charge-pump current and switch to low current after lock detection!

**CPPLL-Based Synthesizer with Lock Detector**

- Critical in determining synthesizer’s performance:
  - Phase noise
  - Spur
  - Settling time
- Extra poles and zeros can be included to control the loop behavior (noise, transient)
- Order of loop filter determines order and stability of the whole loop
Zeroth-Order Loop Filter

\[ G_{LP}(\omega) \]

| \( |H_{\text{open}}(\omega)| \) |

0dB

\( \omega \)

\( \omega_c \)

\( \phi \{H_{\text{open}}(\omega)\} \)

-90°

Zero-order LPF

First-order PLL

First-Order Loop Filter

\[ G_{LP}(\omega) \]

| \( |H_{\text{open}}(\omega)| \) |

0dB

\( \omega \)

\( \omega_c \)

\( \omega_{LP} \)

\( \phi \{H_{\text{open}}(\omega)\} \)

-90°

First-order LPF

Second-order PLL

CPPPL’s Loop Filter

\[ I_{CP} \]

\( \phi_{\text{ref}} \)

\( \phi_{\text{out}} \)

PFD

\( V_C \)

\( R_z \)

\( C_P \)

\( I_{CP} \)

\( C_z \)

Loop Filter – Sampling Noise

- During ON, MOS Switch’s Turn-On Resistance Contributes Thermal Noise \( 4kTR \)

\[ v_n^2 = \int_0^\infty 4kTR_{on} |H(f)|^2 \, df \]

\[ = \int_0^\infty 4kTR_{on} \frac{1}{1 + (\omega R_{on} C_P)^2} \, df \]

\[ = kT \frac{1}{C_P} \]

\[ Ex: v_n \sim 64 \mu V \text{ for } C_P = 1 \text{ pF} \]
Loop Filter

- With Charge-Pump PFD, there exist two poles at zero => need to add zero to ensure stability
- The zero is typically realized using a resistor $R_z$ in series with capacitor $C_z$
- $C_p$ needs to be large enough to minimize $kT/C$ noise
- Due to large ratio of zero and pole, large ratio of $C_p$ and $C_z$ => too large chip area to be integrated on-chip

Active Loop Filter Using Capacitive Multiplication

$$C_{eff} = \frac{R_X}{R_Y} C$$

[Larsson, ISSCC 2001]

- Employ feedback for capacitive multiplication to increase effective capacitance to reduce chip area
- Extra noise from active devices and resistors

Dual-Path Loop Filter

Dual-Path Loop Filter

$$I_{CP}$$

$$B_{ICP}$$

$$C_2$$

$$C_3$$

$$R_1$$

$$C_1$$

$$R_4$$

$$C_4$$

$$V_C$$
**Dual-Path Loop Filter**

\[ H_{LF}(s) = [H_{int}(s) + H_{LPF}(s)]H_4(s) \]

\[ H_{int}(s) = \frac{1}{s(C_2 + C_3)} \approx \frac{1}{sC_3} \]

\[ H_{LPF}(s) = \frac{BR_1}{1 + sC_1R_1}; \quad H_4(s) = \frac{1}{1 + sC_4R_4} \]

\[ H_{LF}(s) = \frac{1}{sC_3} \cdot \frac{1}{1 + s\tau_z} \frac{1}{1 + s\tau_p} = \frac{1}{1 + s\tau_4} \]

\[ \tau_z = R_1(C_1 + BC_3); \quad \tau_p = R_1C_1; \quad \tau_4 = R_4C_4 \]

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**Dual-Path Loop Filter**

- Combine responses of an integrator and a scaled low-pass filter to generate a zero for stability
- By scaling factor B, total capacitance required can be significantly reduced
- Design of low-noise adder could be a limiting factor for noise and power
- Separately-optimized capacitors => Two capacitors need to be large enough for kT/C noise requirement (~1nF each)

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**Dual-Path Loop Filter**

- Unfiltered adder’s noise => noise, power consumption
- Large dynamic range adder needed => Large supply voltage or limited tuning range
- Increase capacitors to reduce the noise source
- Reduce the VCO gain from the noise source to the VCO output
  - Using smaller voltage-controlled capacitors for VCO and larger signal at the filter output
- Tuning signal is limited by the available dynamic range
  - => smaller tuning range
- Trade-off between capacitor size and tuning range
- Outputs of dual paths can drive two varactors directly to eliminate adder to reduce noise and to save power [Lo 2002]
Capacitance-Domain Dual-Path Loop Filter [Lo 2002]

- Use two parallel voltage-controlled capacitors (varactors) to separately control signals in the two paths
- Implement the addition in capacitance domain (by simply connecting two capacitors in parallel)
- Obvious advantage: No voltage adder needed => improve noise, power consumption; lower supply voltage for same tuning range

References

References


